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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,686	11/04/2003	Wolfgang Korber	Q78259	4926

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EXAMINER	
WONG, XAVIER S	

ART UNIT	PAPER NUMBER
2416	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,686	KORBER ET AL.	
	Examiner	Art Unit	
	Xavier Szewai Wong	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23rd March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *Hluchyj NPL*.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 23rd March 2009 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 8, 9, 10, 12, 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Hluchyj et al ("Queueing in High Performance Packet Switching," Hluchyj).

Claim 1: Hluchyj shows a multi-channel network node for routing/switching data from a number of input ports to a number of output ports (pg. 1588, fig. 2a & 2c: input and output queueing), wherein said data is buffered in a memory unit before being passed to a destined output port (pg. 1587, right-col. within para. A, lines 1-4: buffer on its input… awaits access to switch), wherein said multi-channel network node comprises:

said memory unit organized as a number of physical memory queues (pg. 1588, fig. 2a & 2c: input queues 1~N traverse "unit" to output queues 1~N), each queue being physically arranged so that it is physically assigned to an output port to an output port (pg. 1588, fig. 2a – 1~N:1~N queues; fig. 2c – 1~N:1~N queues; pg. 1589, left-col., sec. C lines 1-3: all queueing is done at the outputs of the switch with a separate b packet FIFO provided for each output), and

a switching unit (pg. 1588, fig. 1a: packet switch) for routing said data from the input port to said memory queue which is assigned to the destined output port (pg. 1588, fig. 1b and sec. B: NxN or NbxNb queueing/switching arrangement).

Claim 14: Hluchyj shows a method for routing/switching data from any input port to any of a number of output ports of a multi-channel network node (pg. 1588, fig. 1a: input queues 1~N through switch to output queues 1~N), comprising the steps of:

receiving data from a data channel by a receiver unit (pg. 1588, fig. 2a: inputs 1~N traverses through "receiver unit");

queueing said data in a plurality of memory queues constituting a memory unit (fig. 2a & 2c: input queues / output queues units), wherein each memory queue is physically arranged so that it is physically assigned to an output port (pg. 1588, fig. 2a – 1~N:1~N queues; fig. 2c – 1~N:1~N queues; pg. 1589, left-col., sec. C lines 1-3: all queueing is done at the outputs of the switch with a separate b packet FIFO provided for each output); and

switching/routing the data from the memory queues to the output port the respective memory queue is assigned to (pg. 1593, left-col. sec. C 1st para. – b packet FIFO… destined for tagged output).

Claim 8: Hluchyj teaches a matrix switch (fig. 1a: non-blocking switch is a matrix switch).

Claim 9: Hluchyj teaches the switching unit is provided by a processor controlled by software (fig. 1a: the switch *must* be inherently run by a CPU controlled by codes).

Claim 10: Hluchyj teaches input and output interfaces are assigned to the input (fig. 2a: input interface; pg. 1587, right-col. within para. A, lines 1-4 & 8-10: a separate buffer is placed on each input… addressed to different output) and output ports respectively (fig. 2c: output interface; pg. 1593, left-col. sec. C 1st para. – b packet FIFO… destined for tagged output).

Claim 12: Hluchyj shows the output ports are output ports of the memory unit and are coupled with a switching unit (fig. 2a & 2c input and output queues are coupled to switch in fig. 1a).

Claim 13: Hluchyj shows the output ports are the output ports of the network node (fig. 2c: output queues 1-N of unit / node; *or*, fig. 1a: output queues 1-N of switch node).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 2, 3 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hluchyj et al ("Queueing in High Performance Packet Switching," Hluchyj) in view of Dahlgren et al (US 2003/0115402 A1, Dahlgren).

Claim 2: Hluchyj discloses the claimed invention; yet not specifically "each of said memory queues comprises a number of coherent memory cells." Dahlgren teaches each memory queue comprises a number of coherent memory cells (*abstract*: cache-coherent memory). It would have been obvious to one of ordinary skill in the art when the invention was created to modify the queues or memory of Hluchyj into coherent memory cells as taught by Dahlgren to manage data (in cache) conflicts and maintain consistency between cache and memory.

Claim 3: Hluchyj discloses the claimed invention; yet not specifically "the number of memory cells is resizable in order to redistribute buffer capacity of the memory queues." Dahlgren teaches concept of number of memory cells being resizable ([0064] lines 1-9 & [0066] lines 1-10: memory… dynamic resizing... to a cache coherence protocol). It would have been obvious to one of ordinary skill in the art when the invention was created to modify the queues or memory of Hluchyj into coherent memory cells that are resizable as taught by Dahlgren to balance memory usage.

Claim 15: Hluchyj discloses memory queues; yet not specifically "allocat[ing] coherent memory cells. Dahlgren teaches allocating coherent memory cells ([0064] lines 1-9 & [0066] lines 1-10: memory… *dynamic resizing* (*allocation*)... to a cache coherence protocol). It would have been obvious to one of ordinary skill in the art when the invention was created to modify the queues or memory of Hluchyj into coherent memory cells and allow allocation of the cells as taught by Dahlgren to balance memory usage.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hluchyj et al ("Queueing in High Performance Packet Switching," Hluchyj) in view of Kothary (US 6249528 B1).

Claim 4: Hluchyj discloses the claimed invention; yet not specifically "a re-assembly unit coupled to the input ports of the node and the switch; and a segmentation unit with the memory unit and output ports of the node." Kothary shows in figure *2* a re-assembly unit coupled to a switch unit, which is coupled to a segmentation unit. The re-assembly unit in figure *13* and the segmentation unit in figure *14* both show FIFO buffers (memory units) *152* and *166* respectively (col. 13: 52-67; col. 14: 42-57). It would have been obvious to one of ordinary skill in the art when the invention was created to add the memory unit / re-assembly / segmentation units of Kothary in between the input-switch-output nodes of Hluchyj for cell re-assembly and segmentation purposes.

Claim 5, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hluchyj et al ("Queueing in High Performance Packet Switching," Hluchyj) in view of Yang et al (US 5465331, Yang).

Claim 5: Hluchyj discloses the claimed invention; yet not specifically each memory queue is assigned to a memory agent controlling the operation of the memory queue. Yang each memory queue is assigned to a memory agent controlling the operation of the memory queue (col. 2 lines 1-4: plurality of background buffer controllers each coupled to an individual packet memory). It would have been obvious to one of ordinary skill in the art when the invention was created to implement each memory

queue is assigned to a memory agent controlling the operation of the memory queue as taught by Yang to modify the queues of Hluchyj to provide parallel processing of data.

Claim 6: Hluchyj discloses the claimed invention; yet not very expressively "said memory queues and said memory agents form said switching unit." Yang shows memory queues and memory agents form said switching unit (fig. 4: foreground / background controllers (agents), queue memory QM and connection matrix). It would have been obvious to one of ordinary skill in the art when the invention was created to implement the structure of memory queues and memory agents forming the switching unit as taught by Yang to modify the switch unit of Hluchyj to achieve increased parallel processing of packets.

Claim 7: Hluchyj discloses the claimed invention; yet not very expressively mention "memory agent and memory queues operate asynchronous and in parallel." Yang teaches memory agent and memory queues operate asynchronous and in parallel (col. 7 lines 7-16: FGAM/BGAM agents store packets in any PM queues in parallel). It would have been obvious to one of ordinary skill in the art when the invention was created to implement the memory agent and memory queues operate asynchronous and in parallel as taught by Yang to modify the switch unit of Hluchyj to achieve increased parallel processing of packets.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hluchyj et al ("Queueing in High Performance Packet Switching," Hluchyj) in view of Liebowitz et al (US 5757784, Liebowitz).

Claim 11: Hluchyj teaches the claimed invention; yet not specifically the queues being "burst buffers." Liebowitz teaches in figure *4* the usage of *burst buffer 68* in a fragment assembler/disassembler FAD *66* (col. 4: 19-41). It would have been obvious to one of ordinary skill in the art when the invention was made to apply the burst buffer of Liebowitz to the multi-channel node queues of Hluchyj for efficiently handling different data sizes and formats.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hluchyj et al ("Queueing in High Performance Packet Switching," Hluchyj) in view of Moriwaki et al (EP 0918419 A2, Moriwaki).

Claim 16: Hluchyj teaches the claimed invention; yet has not very specifically shown a network of interactive cascaded multi-channel network nodes. Moriwaki teaches a concept of different levels of inputs and outputs in the ATM switch system from the input highways of the cell distributors to the ATM switches to the output highways of the cell assemblers; therefore, creating a *cascade* of devices operating in a succession of stages (col. *3* lines *52-58* & col. *4* lines *1-46*; fig. *1*). The ATM switch units *exchange (interaction)* cells with other ATM switch units in an N x N switch matrix (col. *6* lines *6-39*; *abstract*; fig. *1*). It would have been obvious to one of ordinary skill in the art when the invention was made to apply the concept of cascaded nodes as taught by Moriwaki to the node structure of Hluchyj for swift inter-node communications.

Response to Arguments

Applicant's arguments with respect to claims 1 and 14 have been considered but are moot in view of the new ground(s) of rejection with new prior arts.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. Jarvis, US 5752255: dynamic cache resizing non-coherent cache memory

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xavier Wong whose telephone number is 571.270.1780. The examiner can normally be reached on Monday through Friday 8:30 am - 6:00 pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571.272.3174. The fax phone number for the organization where this application or proceeding is assigned is 571.273.8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866.217.9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800.786.9199 (IN USA OR CANADA) or 571.272.1000.

/Xavier Szewai Wong/
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12th April 2009

/Seema S. Rao/
Supervisory Patent Examiner, Art Unit 2416